Notice of References Cited	Application/Control No. 09/981,503	Applicant(s)/Patent Under Reexamination HWANG ET AL.	
	Examiner Samuel Broda	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,606,588	08-2003	Schaumont et al.	703/15
	B	US-6,305,001	10-2001	Graef, Stefan	716/12
	C	US-6,216,255	04-2001	Ito et al.	716/6
	D	US-5,870,588	02-1999	Rompaey et al.	703/13
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Krukowski et al, "Simulink/Matlab-to-VHDL Route for Full-Custom/FPGA Rapid Prototyping of DSP Algorithms," Matlab DSP Conference, pp. 1-10 (November 1999)(text available at: http://dolphin.wmin.ac.uk/~artur/pdf/Paper18.pdf)
	V	Garbergs et al, "Implementation of a State Space Controller in a FPGA," IEEE 9th Mediterranean Electrotechnical Conference, Vol. 1, pp. 566-569 (May 1998)
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.